new title is required that is clearly indicative of the invention to which the claims are directed." In response, Applicants have amended the title and have aadditionally amended both the "Technical Field" and the Abstract for consistency.

The Examiner objected to the drawings, alleging that "[t]he drawings fail to show every feature of the invention specified in the claims. Therefore, 'the selected area having approximately the shape of a circular disk approximately centered around the first contact' and 'the flat metal ring' must be shown or the feature(s) canceled from the claim(s). Also, 'a semiconductor chip having a circuit', must be shown or the feature(s) canceled from the claim(s). No new matter should be entered." In response, Applicants have amended the claims to delete the aforementioned features from the claims. Applicants assert that said claim amendments do not narrow the claims, but instead broaden the claims.

The Examiner rejected claim 3 under 35 U.S.C. §112, second paragraph, as allegedly "being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention."

The Examiner rejected claims 1-3, 9 and 20 under 35 U.S.C. §102(b) as being anticipated by Lauffer *et al.* (US 5,665,650).

The Examiner rejected claims 4-8 under 35 U.S.C. §103(a) as being unpatentable over Lauffer et al. (US 5,665,650).

Applicants respectfully traverse the §112, §102 and §103 rejections with the following arguments.

35 U.S.C. §112

The Examiner rejected Claim 3 under 35 U.S.C. §112, second paragraph, alleging "[i]t is not clear to which element of the device the contact pad is parallel."

Applicants respectfully traverse the rejection of claim 3. Applicants contend that claim 3 unambiguously states that the contact pad is parallel to the first contact area of the first metal layer. Accordingly, Applicants respectfully request that the rejection of claim 3 under 35 U.S.C. §112, second paragraph be withdrawn.

35 U.S.C. §102

The Examiner rejected claims 1-3, 9 and 20 under 35 U.S.C. §102(b) as being anticipated by Lauffer *et al.* (US 5,665,650).

The Examiner alleges that "[r]egarding claim 1, Lauffer (e.g. fig. 2) shows an electronic structure comprising:

A substrate having a dielectric layer 14 between a first metal layer 22 and a second metal layer 22;

A contact area located in the first metal layer (the region in contact with the layer 28);

A selected area located on the second metal layer (the area around the through hole);

A microvia cavity located within the selected area and extending through the second metal layer and the dielectric layer;

And a mass of conductive material (28, 32 and 34) forming a layer upon the selected area of the second metal layer and being inside the microvia cavity and being in contact with the first contact area of the first metal layer." The Examiner extends a similar argument with respect to

rejection of Claim 20.

Applicants respectfully contend that Lauffer does not anticipate independent claims 1 and 20, as amended herein, because Lauffer does not teach each and every feature of claims 1 and 20. For example, Lauffer does not teach "a mass of a **single** conductive material forming a layer upon the selected area of the second metal layer and **totally filling** the microvia cavity and being **in contact with the first contact area** of the first metal layer" (emphasis added).

In Lauffer, conductive layer 28 is merely a surface layer to establishing bonding and not a complete fill for the microvia cavity shown in FIG. 1E. Conductive paste 32 fills the area above conductive layer 28, not the entire microvia cavity. In Lauffer, no single conductive material totally fills the microvia cavity and is also in contact with the first contact area of the first metal layer.

Based on the preceding arguments, Applicants respectfully maintain that Lauffer does not anticipate claims 1 and 20, and that claims 1 and 20 are in condition for allowance. Since claims 2-3 and 9 depend from claim 1, Applicants respectfully contend that claims 2-3 and 9 are likewise in condition for allowance.

35 U.S.C. §103

The Examiner rejected claims 4-8 under 35 U.S.C. §103(a) as being unpatentable over Lauffer et al. (US 5,665,650). Since claims 4-8 depend from claim 1, and since Applicants have argued *supra* that claim 1 is in condition for allowance, Applicants respectfully contend that claims 4-8 are likewise in condition for allowance and thus not unpatentable under 35 U.S.C.

§103(a).

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that claims 1-9 and 20 and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below.

Date: 11/27/2002

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Appendix A. Identification of Amended Material

Please amend the Technical Field, beginning on page 1, line 4, as follows:

The invention relates generally to a high semiconductor chip package[ing], and more particularly, to a [method of producing] structure for flip-chip joinable contact pads on a surface of a chip carrier.

Please amend the Abstract as follows:

A flip-chip joinable substrate having non-plated-on contact pads [and a method for making the same]. The substrate has an external metal foil layer upon a dielectric layer upon a patterned internal metal layer having an internal contact area. An area of the external metal foil layer above the internal contact area is selected. A microvia cavity extending to the internal contact area is perforated centrally within the selected area and is filled with a mass of conductive paste forming an external contact pad. The external contact pad is used as an etch mask for removing the adjacent external metal foil.

Please amend claims 1-6, 9, and 20 as follows:

1. (AMENDED) An electronic structure comprising:

a substrate having a dielectric layer between a first metal layer and a second metal layer, the second metal layer being disposed above the first metal layer, the first metal layer having a first contact area, the second metal layer having a selected area disposed above the first contact area;

a microvia cavity within the selected area being disposed through the second metal layer and through the dielectric layer and extending to the first contact area of the first metal layer; and

a mass of a single conductive material forming a layer upon the selected area of the second metal layer and [being inside] totally filling the microvia cavity and being in contact with the first contact area of the first metal layer.

2. (AMENDED) The structure of claim 1, wherein the mass of the single conductive material conformally fills the microvia cavity.

3. (AMENDED) The structure of claim 1, wherein the mass of the single conductive material has a planar surface forming a contact pad located parallel to and opposite the first contact area of the first metal layer.

4. (AMENDED) The structure of claim 1, wherein selected area [has approximately the shape of a circular disk] is approximately centered around the first contact area.

5. (AMENDED) The structure of claim 4, wherein the second metal layer within the selected area [contains a flat metal ring that] is approximately centered around the microvia cavity.

6. (AMENDED) The structure of claim 1, wherein the second metal layer within the selected area [contains a flat metal ring that] is approximately centered around the first contact area.

9. (AMENDED) The structure of claim 1, wherein the mass of the single conductive material comprises at least one of a solder paste, a reflowable solder, a conductive paste, and a conductive adhesive.

20. (AMENDED) An assembly comprising:

a semiconductor chip [having a circuit];

a substrate having a dielectric layer between a first metal layer and a second metal layer, the second metal layer being disposed above the first metal layer, the first metal layer having a first contact area, the second metal layer having a selected area disposed above the first contact area;

a microvia cavity within the selected area being disposed through the second metal layer and through the dielectric layer and extending to the first contact area of the first metal layer; and

a mass of a single conductive material forming a layer upon the selected area of the second metal layer and [being inside] totally filling the microvia cavity and being in contact with the first contact area of the first metal layer[;],

wherein the [circuit] semiconductor chip is electrically connected to the mass of the single conductive material.